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Design considerations for phase dependent voltage contrast technique for application to SEM analysis

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Abstract : A detailed design of the phase Dependent Voltage Contrast technique (PDVC) that can be used for test and evaluation of IC devices has been discussed The technique is easy to implement with a Scanning Electron Microscope (SEM) and operates on the principle that the detector current due to secondary electrons emitted from a device under test (DUT) in a SEM can be modulated by a suitable signal applied to the substrate of the device Large Signal Integration (LSI) failure analysis is enhanced by image contrast of signal phases, and during LSI complex pulse sequencing, proper control of PDVC technique also has the capability to measure internal propagation delays, which was formerly possible only with expensive electron beam blanking techniques.

Keywords : Phase dependent voltage contrast technique, SEM

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1. Introduction

Voltage contrast as applied to SEM analysis is based on the following consideration : The collection of secondary electrons depends greatly on the existence of a net positive potential between the specimen and the Faraday cage of the Everhart-Thornley (E–T) detector [1]. If a potential is applied to regions of a specimen, the potential between the specimen and the collector is altered, thus changing the collection efficiency. Therefore, although equal numbers of secondary electrons may leave each point on the specimen, contrast will be developed because of trajectory effects, dependent on the local nature of the surface potential. A positive potential tends to limit the escape of secondary electrons and causes such a region

in an image to appear dark. A negative potential tends to enhance secondary collection causing bright regions in an image. Voltage contrast is especially useful for the examination of integrated circuits (ICs). A particular aspect of voltage contrast that will be dealt with in this paper is the Phase Dependent Voltage Contrast (PDVC).

2. Design and Discussion

Figure 1 illustrates the block diagram of the technique as outlined in a paper by Younkin [2]. In the present paper, a detailed version of the design for (PDVC / SEM) that can be used for

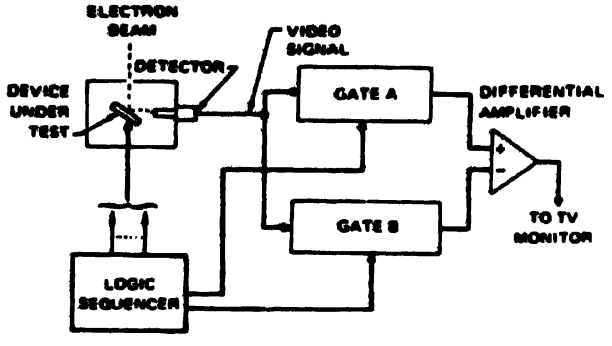

Figure 1. Phase dependent voltage contrast (PDVC) block diagram.

test and evaluation of IC devices has been given. An introductory analysis of the design has been given by Wilkerson [3].

General considerations :

PDVC/SEM operates on the principle that the detector current due to secondary electrons emitted from a device under test (DUT) in a SEM can be modulated by a suitable signal applied to the substrate of the device. This modulation signal should be a rectangular waveform restricted in voltage to within the supply limits of the device. The electron beam in the SEM may scan the device in either slow-scan or TV-scan rates and the technique proposed must provide for these modes in such a way as to give an easily interpretable video output signal to an external monitor. It would be desirable to make provisions for viewing either modulated of unmodulated video, normal or inverse video mode, and DC or AC modulation to the device. It is anticipated that video gate delay with respect to device modulation may be required from time to time, and also that various ratios of modulation and gatings may be needed in order to view device performance to the best advantage. Also, it would be desirable to provide for a full range of gated cycle times. All of these features have been incorporated into the design discussed in this paper.

Theory of operation :

The individual units of the PDVC/SEM controller are described in this sub-section.

(i) Power supply (Figure 2) : The controller is designed to operate from an external bipolar symmetric DC supply providing between 15 and 18 VDC against ground.

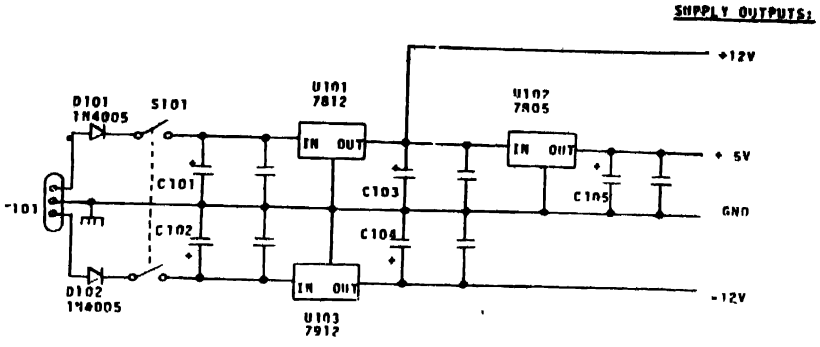

Figure 2. PDVC/SEM controller, power supply schematic.

The Unit will not operate with less than 14 V and will overheat with greater than 20 V. Diodes D101 and D102 prevent damage due to reverse connections.

(ii) Master clock and range dividers (Figure 3) : U201 is a dual oscillator providing an asymmetric rectangle at 20 MHz. One oscillator is disabled and can be used for a

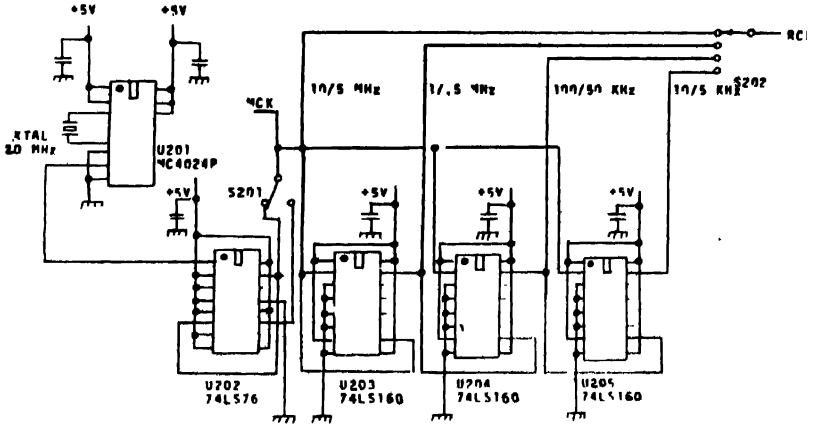

Figure 3. PDVC/SEM controller, master clock and range dividers.

colorburst reference at 3579.545 KHz if desired. The 20 MHz signal is divided and symmetrized by the flipflops of U202 to give the master clock MCK which is 10 MHz or 5 MHz depending on the position of NORMAL/HALFRATE switch S201. Cascaded decade dividers U203, U204 and U205 provide counting triggers to the range clock RCK through S202, giving eight selectable cycle times. Because of the 100 : 1 vernier (see part *iii*), these signals are ranged from 5 KHz to10 MHz.

(iii) *100 division timing vernier (Figure 4) :* The vernier consists of cascaded decade dividers U301 and U302. It provides a two digit BCD timing word defined by

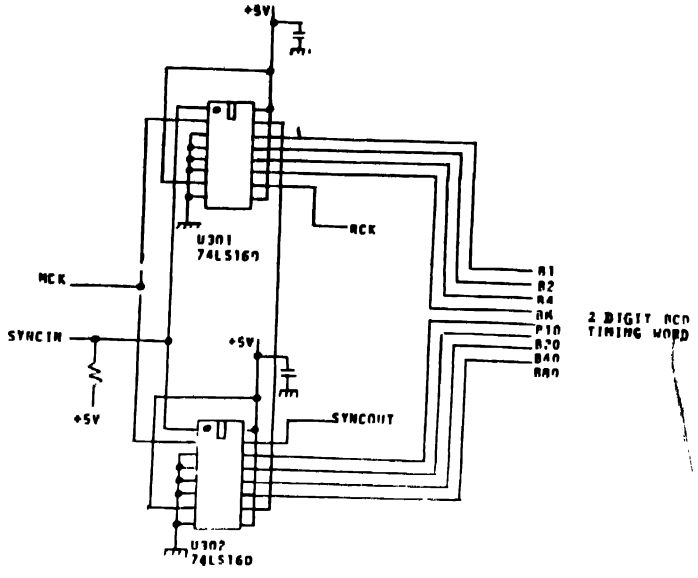

Figure 4. PDVC/SEM controller, 100 division timing vernier

signals B1 through B80. The weight of each line is given by its name, *viz.*, B20 has weight = 20. The vernier steps on the trailing-edge of RCK and is synchronized by MCK.

(iv) *Modulation and gate timing (Figure 5) :* There are four of these units, a generic one of which is shown in Figure 5. Each consists of two four-bit cascaded comparators

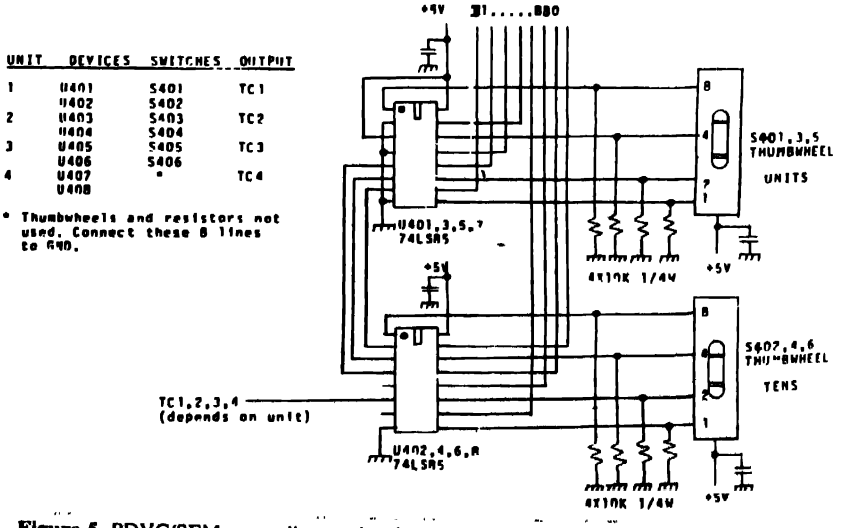

Figure 5. PDVC/SEM controller, mod and gate timing (one of four units shown).

output a pulse when ever the word on B1–B80 matches the word (00–99) set on the thumbwheel switch pair associated with that unit. However, unit # 4 has no switches, its word being fixed at 00 so that the device modulation waveform always comes up at the start of the cycle. Unit # 3, MOD DUTY FACTOR, sets the time when the modulation waveform comes back down. Unit # 1, A GATE DELAY, sets the time when the A gate comes on, and Unit # 2, END A GATE sets the time when the A gate goes off.

(v) *Modulation and gating latch gates (Figure 6)* : These gates consist of four-input NAND gates whose outputs GLS, GLR, MLS, and MLR are brought low by the word coincidences appearing on the lines TC1–TC4 respectively. These gates are required for two reasons : (a) the coincidence pulses are of incorrect polarity to set the latches (see Figure 7); (b) set and reset signals to the latches may not appear simultaneously, as would be the case, *e.g.*, if A GATE DELAY = END A GATE or if MOD DUTY FACTOR = 00. If it is desired to have the A gate on all the time,

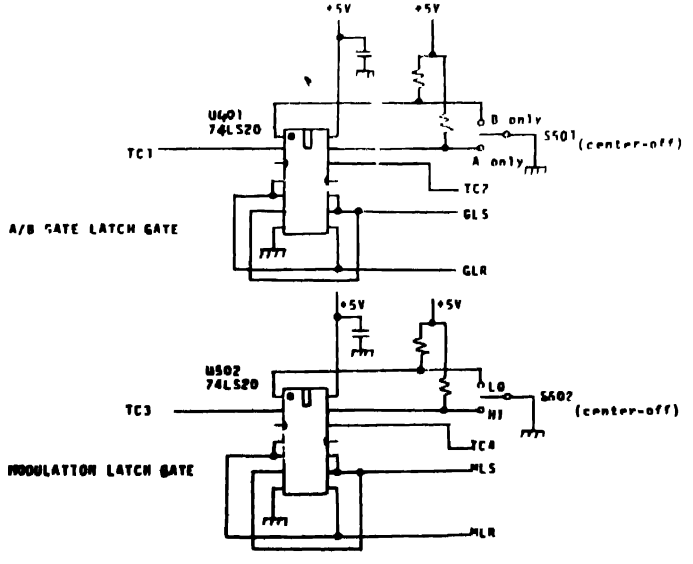

Figure 6. PDVC/SEM controller, mod and gate latches–gates

set S501 to A ONLY (similarly for B on always). If only one modulation level is to be applied, set S502 accordingly, else place it in center position.

(vi) *Modulation and gate latches and A/B gate (Figure 7)* : The flipflops of U601 control the states of the CMOS analog switch U602 and also provide the rectangular modulation signal to the device modulator (see Figure 8). Switch S601, NORM/INVERSE VIDEO, does not function like its counterpart in the SEM because this switch merely exchanges the roles of the A and B gates. The same

effect could have been obtained by exchanging the values of A GATE DELAY and END A GATE, but using S601 is more convenient.

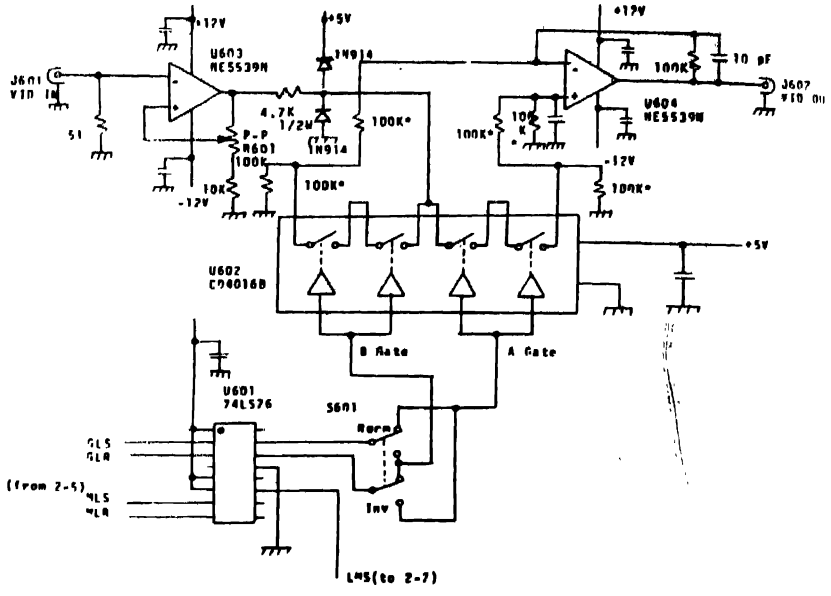

Figure 7. Modulation and gate latches and A/B gate.

Figure 7 shows the arrangement for standard TV positive video, 5 MHz bandwidth, and 50 ohm input impedance. The VIDEO GAIN control R601 gives a gain of 1 to 10, but the signal at the output of U603 is limited between 0 and 5 V to protect U602. The A and B analog switches are in series tandem to provide about 80 db (10,000 : 1) isolation between the channels. The differential amplifier U604 drives the VIDEO OUTPUT at about 50 OHMS and 5 MHz bandwidth. A small roll off is provided to reduce switching transients.

(vii) *Device modulator (Figure 8):* The four opamps of U701 condition the TTL modulation signal from U601 so that it varies between two adjustable voltages in order to bias the device substrate properly. The control R701, P–P MOD, controls the peak to peak amplitude and the control R702, MOD LEVEL, controls the DC reference level of the signal at MOD OUT. This signal can source about 10 ma at a 500 KHz bandwidth. If necessary, video opamps can be substituted for U701 to improve the edge contrast on the 100 KHz range setting. U701B and U701C provide upper and lower clamp levels, respectively, to protect the device under test. With S701 set as shown, these levels are 4.35 V and 0.65 V. Provisions are shown for other clamp references to be applied at J701. Additional details of the design are given in the final report by Kadaba [4].

Plate I

Figure 9. SEM micrographs of the oxide layer from an aged anode foil of an electrolytic capacitor : (a) pattern without the PDVC attachment, (b) pattern with the PDVC attachment.

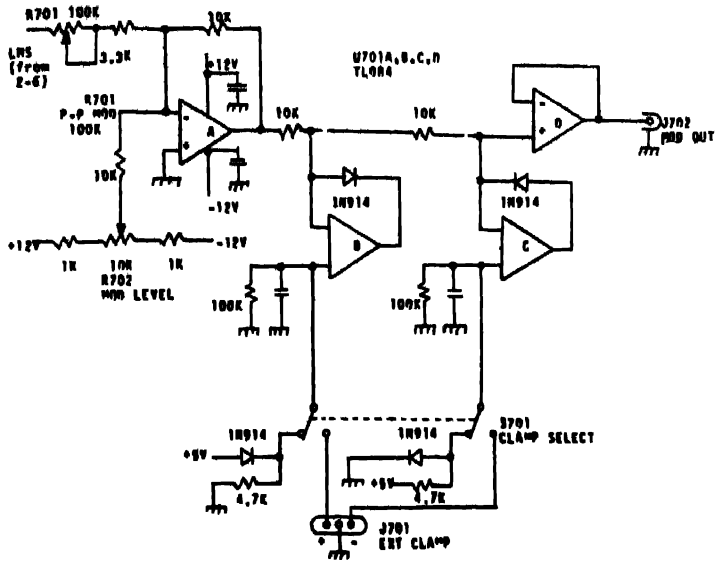

Figure 8. Device modulator. J701 = 3 terminal jack or terminal strip to suit.

3. Results

The test results using a JEOL Scanning Electron Microscope are shown in Figures 9(a) and 9(b) the SEM micrographs are those of the anodic oxide layer of an aged aluminum electrolytic capacitor. Figure 9(a) is the pattern without interfacing the SEM with the PDVC controller, where as Figure 9(b) is the result of interfacing the SEM with the PDVC controller described in detail in this paper. As can be seen the SEM micrograph with the PDVC attachment–Figure 9(b)–has better clarity and shows more details of the "spaghetti-like" tubular structure. The width of these tubular patterns is estimated to be of the order of 50 to 80 nm.

So in conclusion, Scanning Electron Microscope images of better quality should result when the above design is interfaced with a suitable SEM.

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